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To: Assistant Commissioner for Patents
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Sir: Transmitted herewith for filing is the patent application of:

Inventor: E. HASE et al (See Attached List)

For:
HIGH FREQUENCY CIRCUIT MODULE AND COMMUNICATION DEVICE

Enclosed are:

- [X] 11 Sheets of Drawings
- [ ] This application is being filed without an executed Declaration.
- [X] Priority is claimed from Japanese Application No. 11-275730 filed September 29, 1999. ☐ A certified copy is attached herewith.
- [X] Copies of the disclosure documents listed on the attached PTO 1449 form and ☒ discussed in the specification or ☐ attached Information Disclosure Statement.
- [ ] A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.
- [X] Specification: Abstract X, Description 25 pages; and 16 claim(s).
- [ ] Preliminary Amendment.
- [X] Executed Declaration.

The filing fee is calculated as shown below:

For:	No. Filed	No. Extra
Basic Fee		
Total Claims	16 -20=	* 0
Indep Claims	4 - 3 =	* 1
☐ Multiple Dependent Claim (s)		

* If difference is less than zero then enter '0' in second column

Small Entity

Rate	Fee
	$ 345
x 9	$
x 39	$
+ 130	$
Total	$

OR

Large Entity

Rate	Fee
	$ 690
x 18	$ 0
x 78	$ 78
+ 260	$ 0
Total	$ 768

- [X] A check in the amount of $ 768.00 is enclosed for the filing fee.
- [X] The Commissioner is hereby authorized to charge any additional fees that may be required to Deposit Account No. 50-1417.

Respectfully Submitted,

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Title of the Invention

HIGH FREQUENCY CIRCUIT MODULE AND COMMUNICATION DEVICE

Inventors

Eiichi HASE
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TITLE OF THE INVENTION

HIGH FREQUENCY CIRCUIT MODULE AND COMMUNICATION DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a high frequency circuit module and a communication device such as a mobile wireless terminal and a pocket telephone using it.

Description of the Prior Art

The miniaturization and the enhancement of the efficiency of power of a high frequency circuit module used for a mobile wireless terminal, a pocket telephone and others in view of the mountability and talk time have been an important objective.

For a high frequency circuit module used for a communication device such as conventional type mobile wireless terminal and pocket telephone, the one using a single layer or multi-layer dielectric substrate is known.

An example of a high frequency circuit module using a single layer dielectric substrate is shown in the proceeding of the 1996 Institute IEIC Spring Conference C-86, "A Power Amplifier Using Single Layer Alumina Substrate with Thin-Film Resistors and Capacitors for North American Digital Phone System" (hereinafter called first conventional technique). According to the first conventional technique, a

transmission line which is a distributed element, a lumped constant element such as a resistor, a capacitor and an inductor and a semiconductor element are formed on the same surface of a dielectric substrate to compose an input-output matching circuit and a power amplifier. A high frequency signal is transmitted to an external device by a high frequency signal electrode provided to the surface of the dielectric substrate. The earth electrode of the semiconductor element provided to the surface of the dielectric substrate and an earth electrode on the reverse side are connected via a through-hole.

Also, an example of a high frequency circuit module using a multi-layer (two-layer) dielectric substrate is shown in the proceeding of the 1997 Institute IEIC Conference Electronics Society C-2-14, "1.9 GHz RF Front-End Module Using A Ceramics Substrate" (hereinafter called second conventional technique). According to the second conventional technique, a transmission line which is a distributed constant element, an input-output matching circuit composed of a lumped constant element such as a resistor, a capacitor and an inductor and a semiconductor element are formed on the same surface of a dielectric substrate to compose a high frequency circuit module. A high frequency signal electrode provided to the surface of a first layer of the dielectric substrate and a high frequency signal

electrode on the reverse side of a second layer are connected via wiring provided to the surface of the second layer through a through-hole. The earth electrode of the semiconductor element provided to the surface of the first layer of the dielectric substrate and an earth electrode on the reverse side are connected via a through-hole. The order of the layers of the dielectric substrate are counted as a first layer, a second layer, a third layer, --- from the surface to the reverse side.

SUMMARY OF THE INVENTION

Referring to Figs. 9 to 11, relationship between the miniaturization and the enhancement of the efficiency of power in the first conventional type technique will be described below.

Fig. 9 is a general schematic sectional view showing a transmission line formed on a single layer dielectric substrate. A conductor 43 on the surface, a dielectric substrate 44 and ground metal on the reverse side 45 forms a transmission line.

Fig. 10 shows calculated values of transmission loss at the frequency of 1.9 GHz when the relative dielectric constant of the dielectric substrate 44 is 8.1 and the thickness of the dielectric substrate 44 is varied from 0.1 mm to 3.0 mm. Curves 1 to 3 show cases in which the width of the conductor 43 forming a transmission line is respectively 0.1 mm, 0.2 mm and

0.5 mm. As clear from Fig. 10, in the cases of any width of the conductor 43, as the dielectric substrate 44 becomes thick, the transmission loss has a tendency to become small.

Fig. 11 shows calculated values of transmission loss at the frequency of 1.9 GHz when the relative inductivity of the dielectric substrate 44 is 8.1 and the width of the conductor 43 forming a transmission line is varied from 0.02 mm to 3.0 mm. Curves 1 to 3 show cases in which the thickness of the dielectric substrate 44 is respectively 0.15 mm, 0.3 mm and 0.6 mm. As clear from Fig. 11, in the cases of any thickness of the dielectric substrate 44, the transmission loss decreases as the conductor 43 forming a transmission line becomes wide, becomes minimum in a range in which the width of the conductor 43 is 0.3 to 0.7 mm and increases when the conductor 43 becomes wider.

As clear from the above description, to reduce transmission loss, it is required to thicken the dielectric substrate 44 and widen the conductor 43 and the miniaturization of the high frequency circuit module has a limit.

Next, referring to Figs. 12 to 14, relationship between the miniaturization and the enhancement of the efficiency of power in the second conventional type technique will be described.

Fig. 12 is a general schematic sectional view showing a transmission line formed on a two-layer

dielectric substrate. A conductor 46, a dielectric substrate 47, ground metal 48 on the reverse side and ground metal 49 on the surface forms a transmission line.

Fig. 13 shows calculated values of transmission loss at the frequency of 1.9 GHz when the relative dielectric constant of the dielectric substrate 47 is 8.1 and the thickness of the dielectric substrate 47 is varied from 0.1 mm to 3.0 mm. Curves 1 to 3 show cases in which the width of the conductor 46 forming a transmission line is respectively 0.1 mm, 0.2 mm and 0.5 mm. As clear from Fig. 13, in the cases of any width of the conductor 46, as the dielectric substrate 47 becomes thick, the transmission loss becomes small.

Fig. 14 shows calculated values of transmission loss at the frequency of 1.9 GHz when the relative inductivity of the dielectric substrate 47 is 8.1 and the width of the conductor 46 forming a transmission line is varied from 0.02 mm to 3.0 mm. Curves 1 to 3 show cases in which the thickness of the dielectric substrate 47 is respectively 0.15 mm, 0.3 mm and 0.6 mm. As clear from Fig. 14, in the cases of any thickness of the dielectric substrate 47, as the conductor 46 forming a transmission line becomes wide, the transmission loss has a tendency to become small.

As clear from the above description, to reduce transmission loss, it is required to thicken the dielectric substrate 47 and widen the conductor 46 and

the miniaturization of the high frequency circuit module has a limit.

The object of this invention is to provide a high frequency circuit module which can be more miniaturized and a communication device using it.

To achieve the object, a high frequency circuit module according to this invention uses a two or more-layer dielectric substrate and the thickness of the dielectric substrate between a conductor forming the transmission line of a matching circuit on the side of input or output and ground metal is composed of two or more layers.

Concretely, to thicken a dielectric substance that ranges between the conductor forming the transmission line of the matching circuit on the side of input or output and the ground metal, the ground metal provided to the dielectric substrate between them is formed in the shape in which a part is hollowed out so that a part opposite to the conductor is included.

As a required part can be thickened without varying the thickness of the whole dielectric substrate, the transmission loss can be reduced, and a high frequency circuit module and a communication device using it can be miniaturized.

The above-mentioned and others features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an exploded view showing a high frequency circuit module equivalent to a first embodiment of the invention;

Fig. 2 is a sectional view showing the high frequency circuit module equivalent to the first embodiment of the invention;

Fig. 3 shows an equivalent circuit as the whole amplifier of the high frequency circuit module equivalent to the first embodiment of the invention;

Fig. 4 shows calculated values of the loss of a matching circuit on the output side of a conventional high frequency circuit module;

Figs. 5 are an exploded view and a sectional view showing a high frequency circuit module equivalent to a second embodiment of the invention;

Figs. 6 are an exploded view and a sectional view showing a high frequency circuit module equivalent to a third embodiment of the invention;

Figs. 7 are an exploded view and a sectional view showing a high frequency circuit module equivalent to a fourth embodiment of the invention;

Figs. 8 are an exploded view and a sectional view showing a high frequency circuit module equivalent to a fifth embodiment of the invention;

Fig. 9 is a sectional view showing a transmission line formed on a single layer dielectric substrate;

Fig. 10 shows calculated values of the high frequency loss of the transmission line formed on the single layer dielectric substrate in case the thickness of the dielectric substrate is varied;

Fig. 11 shows calculated values of the high frequency loss of the transmission line formed on the single layer dielectric substrate in case the width of a conductor is varied;

Fig. 12 is a sectional view showing a transmission line formed on a two-layer dielectric substrate;

Fig. 13 shows calculated values of the high frequency loss of the transmission line formed on the two-layer dielectric substrate in case the thickness of the dielectric substrate is varied;

Fig. 14 shows calculated values of the high frequency loss of the transmission line formed on the two-layer dielectric substrate in case the width of a conductor is varied;

Fig. 15 is a block diagram showing a high frequency unit of a mobile wireless terminal; and

Fig. 16 is a part layout drawing showing the high frequency unit of the mobile wireless terminal.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The invention will be detailedly described based upon embodiments below.

First Embodiment

Fig. 1 is an exploded view showing a high

frequency circuit module equivalent to a first embodiment. On the surface of a first-layer dielectric substrate 1, a matching circuit on the input side composed of conductor line 2 and chip capacitors 3, 4 and 5 and a matching circuit on the output side composed of conductor line 9 and chip capacitors 10, 11 and 12 are formed. The chip capacitor 3 is connected to an input terminal 8, the chip capacitor 4 is connected to an earth terminal 6, the chip capacitor 5 is connected to an earth terminal 7, the chip capacitor 10 is connected to an output terminal 15, the chip capacitor 11 is connected to an earth terminal 13 and the chip capacitor 12 is connected to an earth terminal 14. Further, a through-hole 17 piercing the first-layer dielectric substrate 1 is provided to the dielectric substrate. A semiconductor chip 16 is bonded to ground metal 19 provided on a second-layer dielectric substrate 18 via the through-hole 17.

The conductor line 2 on the surface of the first-layer dielectric substrate 1 is connected to one end of conductor line 25 provided on the surface of a third-layer dielectric substrate 24 via a through-hole 120 provided to the first-layer dielectric substrate 1 and a through-hole 20 provided to the second-layer dielectric substrate 18. The other end of the line 25 is connected to a terminal 26 provided on the surface of the first-layer dielectric substrate 1 via a through-hole 21 provided to the second-layer dielectric

substrate 18 and a through-hole 121 provided to the first-layer dielectric substrate 1.

Also, the conductor line 9 on the surface of the first-layer dielectric substrate 1 is connected to one end of a conductor line 31 provided on the surface of a fourth-layer dielectric substrate 30 via a through-hole 122 provided to the first-layer dielectric substrate 1, a through-hole 22 provided to the second-layer dielectric substrate 18 and a through-hole 27 provided to the third-layer dielectric substrate 24. The other end of the conductor line 31 is connected to a terminal 32 provided on the surface of the first-layer dielectric substrate 1 via a through-hole 28 provided to the third-layer dielectric substrate 24, a through-hole 23 provided to the second-layer dielectric substrate 18 and a through-hole 123 provided to the first-layer dielectric substrate 1.

The semiconductor chip 16 is bonded to the conductor lines 2 and 9 on the surface of the first-layer dielectric substrate 1. The ground metal 19 on the surface of the second-layer dielectric substrate 18 to which the semiconductor chip 16 is bonded is connected to ground metal 29 provided on the surface of the third-layer dielectric substrate 24, ground metal 33 provided on the surface of the fourth-layer dielectric substrate 30 and ground metal 34 provided on the reverse side of the fourth-layer dielectric substrate 30 via a through-hole 151 provided to the

second-layer dielectric substrate 18, a through-hole 152 provided to the third-layer dielectric substrate 24, a through-hole 153 provided to the fourth-layer dielectric substrate 30 and a through-hole 154 provided to the ground metal 34 on the reverse side of the fourth-layer dielectric substrate 30. Each rectangular frame respectively surrounding the through-holes 151, 152, 153 and 154 shows an area where the semiconductor chip 16 is to be installed.

A part 35 of the ground metal 19 on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 9 of the matching circuit on the output side on the surface of the first-layer dielectric substrate 1 is included. The ground metal 19 is connected to the ground metal 29, 36 and 37 provided on the surface of the third-layer dielectric substrate 24, the ground metal 33, 38 and 39 provided on the surface of the fourth-layer dielectric substrate 30 and the ground metal 34 provided on the reverse side of the fourth-layer dielectric substrate 30 via through-holes (no reference number) provided in the periphery of the second-, third- and fourth-layer dielectric substrates 18, 24 and 30 and through-holes (no reference number) provided in the periphery of the ground metal 34 provided on the reverse side of the fourth-layer dielectric substrate 30.

In this embodiment, each ground metal and each through-hole are connected by forming each ground metal

by copper and embodying copper in each through-hole.

In this embodiment, the first-layer dielectric substrate 1 and the second-layer dielectric substrate 18 continue between the conductor line 9 and the ground metal 29, and for the thickness between both, the thickness of the second-layer dielectric substrate 18 is added to that of the first-layer dielectric substrate 1. Therefore, the thickness between the conductor line 9 and the ground metal 29 can be thicker than the thickness of only the first-layer dielectric substrate 1 or the second-layer dielectric substrate 18 and the transmission loss can be reduced.

In this embodiment, the terminals 8 and 15 via which a high frequency signal is input/output and the terminals 26 and 32 via which voltage is applied to the semiconductor chip 16 are provided on the surface of the first-layer dielectric substrate 1, however, for example, a terminal via which a high frequency signal is input/output may be also provided on the surface of the first-layer dielectric substrate 1 and a terminal via which voltage is applied to the semiconductor chip 16 may be also provided on the reverse side of the fourth-layer dielectric substrate 30. Also, a terminal via which a high frequency signal is input/output and a terminal via which voltage is applied to the semiconductor chip 16 may be also provided on the reverse side of the fourth-layer dielectric substrate 30. And the number of terminals is also not

particularly limited.

Fig. 2 is a sectional view viewed along a line II-II in case the dielectric substrates shown in Fig. 1 are assembled. The dielectric substrate in the part 35 can be thicker than the first-layer dielectric substrate 1, the second-layer dielectric substrate 18, the third-layer dielectric substrate 24 and the fourth-layer dielectric substrate 30 by providing the part 35 formed by removing a part of the ground metal 19 on the surface of the second-layer dielectric substrate 18.

Fig. 3 shows an equivalent circuit of a single-stage amplifier of the high frequency circuit module shown in Fig. 1. It includes a matching circuit on the input side composed of the conductor line 2, chip capacitors 3, 4 and 5, a line 25 that applies power supply voltage to the semiconductor chip 16 including bonding wire, a power supply voltage terminal 26 and an input terminal 8 and a matching circuit on the output side composed of a conductor line 9, chip capacitors 10, 11 and 12, a line 31 that applies power supply voltage to the semiconductor chip 16 including bonding wire, a power supply voltage terminal 32 and an output terminal 15. The conductor line 2 is composed of a conductor lines 2a, 2b and 2c and the conductor line 9 is composed of conductor lines 9a, 9b and 9c.

Fig. 4 shows the loss of the matching circuit in case the equivalent circuit of the matching circuit on the output side shown in Fig. 3 is composed of a

single layer dielectric substrate 44 as shown in Fig. 9, the output impedance of the semiconductor chip 16 including bonding wire is 1 to 100 Ω, load impedance is 50 Ω, the relative inductivity of the dielectric substrate 44 is 8.1, the width of the conductor line 9 formed on the dielectric substrate 44 is 0.3 mm, the dielectric loss tangent tanδ of the dielectric substrate 44 is 0.017, the length of the conductor lines 9a, 9b and 9c and the values of the chip capacitors 10, 11 and 12 are optimized so that they are matched at the frequency of 1.9 GHz. As shown in Fig. 4, curves 1, 2 and 3 show calculated values in case the thickness of the dielectric substrate 44 is respectively 0.15 mm, 0.3 mm and 0.6 mm. As clear from Fig. 4, as the dielectric substrate 44 forming the conductor line 9 becomes thick, the loss of the matching circuit has a tendency to become small. For example, when the output impedance of the semiconductor chip 16 including bonding wire is 10 Ω, the loss of the matching circuit is 0.16 dB in case the thickness of the dielectric substrate 44 is 0.15 mm, however, when the thickness of the dielectric substrate 44 is 0.3 mm, the loss of the matching circuit is 0.13 dB and when the thickness of the dielectric substrate 44 is 0.6 mm, the loss of the matching circuit is reduced up to 0.1 dB.

Second Embodiment

Fig. 5A is an exploded view showing a high

frequency circuit module equivalent to a second embodiment and Fig. 5B is a sectional view viewed along a line VB-VB in case the high frequency circuit module shown in Fig. 5A is assembled. A matching circuit on the input side composed of a conductor line 2 and chip capacitors 3, 4 and 5 is formed on a first-layer dielectric substrate 1, the chip capacitor 3 is connected to an input terminal 8, the chip capacitor 4 is connected to an earth terminal 6 and the chip capacitor 5 is connected to an earth terminal 7. The input terminal 8 is connected to a terminal 8c provided by removing ground metal formed on the reverse side of a third-layer dielectric substrate 24 via a through-hole 8a provided to a second-layer dielectric substrate 18 and a through-hole 8b provided to the third-layer dielectric substrate 24. Further, a matching circuit on the output side composed of a conductor line 9 and chip capacitors 10, 11 and 12 is formed, the chip capacitor 10 is connected to an output terminal 15, the chip capacitor 11 is connected to an earth terminal 13 and the chip capacitor 12 is connected to an earth terminal 14. The output terminal 15 is connected to a terminal 15c provided by removing ground metal formed on the reverse side of the third-layer dielectric substrate 24 via a through-hole 15a provided to the second-layer dielectric substrate 18 and a through-hole 15b provided to the third-layer dielectric substrate 24.

To bond a semiconductor chip 16 to ground metal

19 provided on the surface of the second-layer dielectric substrate 18, a dielectric substance is removed and a hole 17 that pierces the dielectric substrate is provided to the first-layer dielectric substrate 1. The conductor line 2 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 26. Also, the conductor line 9 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 32.

The semiconductor chip 16 is bonded to the conductor lines 2 and 9 provided on the surface of the first-layer dielectric substrate 1. The ground metal 19 formed on the surface of the second-layer dielectric substrate 18 to which the semiconductor chip 16 is bonded is connected to ground metal 29 provided on the surface of the third-layer dielectric substrate 24 and ground metal 34 formed on the reverse side of the third-layer dielectric substrate 24 via through-holes in a part where the semiconductor chip 16 is bonded.

A part 35 of the ground metal 19 formed on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 9 of the matching circuit on the output side formed on the surface of the first-layer dielectric substrate 1 is included. The ground metal 19 is connected to the ground metal 29 and 34 respectively formed on the surface and on the reverse side of the third-layer dielectric substrate 24 via through-holes in the

periphery of the dielectric substrate.

Third Embodiment

Fig. 6A is an exploded view showing a high frequency circuit module equivalent to a third embodiment and Fig. 6B is a sectional view viewed along a line VIB-VIB in case the high frequency circuit module shown in Fig. 6A is assembled. A matching circuit on the input side composed of a conductor line 2 and chip capacitors 3, 4 and 5 is formed on the surface of a first-layer dielectric substrate 1, the chip capacitor 3 is connected to an input terminal 8, the chip capacitor 4 is connected to an earth terminal 6 and the chip capacitor 5 is connected to an earth terminal 7. The input terminal 8 is connected to a terminal 8c provided by removing ground metal formed on the reverse side of a third-layer dielectric substrate 24 via a through-hole 8a provided to a second-layer dielectric substrate 18 and a through-hole 8b provided to the third-layer dielectric substrate 24. Further, a matching circuit on the output side composed of a conductor line 9 and chip capacitors 10, 11 and 12 is formed, the chip capacitor 10 is connected to an output terminal 15, the chip capacitor 11 is connected to an earth terminal 13 and the chip capacitor 12 is connected to an earth terminal 14. The output terminal 15 is connected to a terminal 15c provided by removing ground metal 34 formed on the reverse side of the third-layer dielectric substrate 24 via a through-hole

15a provided to the second-layer dielectric substrate 18 and a through-hole 15b provided to the third-layer dielectric substrate 24.

To bond a semiconductor chip 16 to ground metal 19 provided on the surface of the second-layer dielectric substrate 18, a dielectric substance is removed and a hole 17 that pierces the dielectric substrate is provided to the first-layer dielectric substrate 1. The conductor line 2 provided on the first-layer dielectric substrate 1 is connected to a terminal 26. Also, the conductor line 9 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 32.

The semiconductor chip 16 is bonded to the conductor lines 2 and 9 provided on the surface of the first-layer dielectric substrate 1. The ground metal 19 formed on the surface of the second-layer dielectric substrate 18 to which the semiconductor chip 16 is bonded is connected to ground metal 29 and 34 provided on the surface and on the reverse side of the third-layer dielectric substrate 24 via through-holes in a part where the semiconductor chip 16 is bonded.

A part 35 of the ground metal 19 formed on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 9 of the matching circuit on the output side formed on the surface of the first-layer dielectric substrate 1 is included. Further, a part 40 of the ground metal 29

on the surface of the third-layer dielectric substrate 24 is removed so that a part opposite to the conductor line 9 is included. The ground metal 19 and 29 are connected to each other via through-holes in the periphery of the dielectric substrate and is also connected to the ground metal 34 formed on the reverse side of the third-layer dielectric substrate 24.

Fourth Embodiment

Fig. 7A is an exploded view showing a high frequency circuit module equivalent to a fourth embodiment and Fig. 7B is a sectional view viewed along a line VIIB-VIIB in case the high frequency circuit module shown in Fig. 7A is assembled. A matching circuit on the input side composed of a conductor line 2 and chip capacitors 3, 4 and 5 is formed on the surface of a first-layer dielectric substrate 1, the chip capacitor 3 is connected to an input terminal 8, the chip capacitor 4 is connected to an earth terminal 6 and the chip capacitor 5 is connected to an earth terminal 7. The input terminal 8 is connected to a terminal 8c provided by removing ground metal formed on the reverse side of a third-layer dielectric substrate 24 via a through-hole 8a provided to a second-layer dielectric substrate 18 and a through-hole 8b provided to the third-layer dielectric substrate 24. Further, a matching circuit on the output side composed of a conductor line 9 and chip capacitors 10, 11 and 12 is formed, the chip capacitor 10 is connected to an output

terminal 15, the chip capacitor 11 is connected to an earth terminal 13 and the chip capacitor 12 is connected to an earth terminal 14. The output terminal 15 is connected to a terminal 15c provided by removing ground metal formed on the reverse side of the third-layer dielectric substrate 24 via a through-hole 15a provided to the second-layer dielectric substrate 18 and a through-hole 15b provided to the third-layer dielectric substrate 24.

To bond a semiconductor chip 16 to ground metal 19 provided on the surface of the second-layer dielectric substrate 18, a dielectric substance is removed and a hole 17 that pierces the dielectric substrate is provided to the first-layer dielectric substrate 1. The conductor line 2 provided on the first-layer dielectric substrate 1 is connected to a terminal 26. Also, the conductor line 9 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 32.

The semiconductor chip 16 is bonded to the conductor lines 2 and 9 provided on the surface of the first-layer dielectric substrate 1. The ground metal 19 formed on the surface of the second-layer dielectric substrate 18 to which the semiconductor chip 16 is bonded is connected to ground metal 29 and 34 provided on the surface and on the reverse side of the third-layer dielectric substrate 24 via through-holes in a part where the semiconductor chip 16 is bonded.

A part 41 of the ground metal 19 on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 2 of the matching circuit on the input side on the surface of the first-layer dielectric substrate 1 is included. Further, a part 35 of the ground metal 19 on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 9 of the matching circuit on the output side is included. The dielectric substrate in the removed part can be thicker than the first-layer dielectric substrate 1, the second-layer dielectric substrate 18 or the third-layer dielectric substrate 24. The ground metal 19 is connected to the ground metal 29 and 34 formed on the surface and on the reverse side of the third-layer dielectric substrate 24 via through-holes in the periphery of the dielectric substrate.

Fifth Embodiment

Fig. 8A is an exploded view showing a high frequency circuit module equivalent to a fifth embodiment and Fig. 8B is a sectional view viewed along a line VIIIB-VIIIB in case the high frequency circuit module shown in Fig. 8A is assembled. A matching circuit on the input side composed of a conductor line 2 and chip capacitors 3, 4 and 5 is formed on the surface of a first-layer dielectric substrate 1, the chip capacitor 3 is connected to an input terminal 8, the chip capacitor 4 is connected to an earth terminal

6 and the chip capacitor 5 is connected to an earth terminal 7. The input terminal 8 is connected to a terminal 8c provided by removing ground metal formed on the reverse side of a second-layer dielectric substrate 18 via a through-hole 8a provided to the second-layer dielectric substrate 18. Further, a matching circuit on the output side composed of a conductor line 9 and chip capacitors 10, 11 and 12 is formed, the chip capacitor 10 is connected to an output terminal 15, the chip capacitor 11 is connected to an earth terminal 13 and the chip capacitor 12 is connected to an earth terminal 14. The output terminal 15 is connected to a terminal 15c provided by removing ground metal formed on the reverse side of the second-layer dielectric substrate 18 via a through-hole 15b provided to the second-layer dielectric substrate 18.

To bond a semiconductor chip 16 to ground metal 19 provided on the surface of the second-layer dielectric substrate 18, a dielectric substance is removed and a hole 17 that pierces the dielectric substrate is provided to the first-layer dielectric substrate 1. The conductor line 2 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 26. Also, the conductor line 9 provided on the surface of the first-layer dielectric substrate 1 is connected to a terminal 32.

The semiconductor chip 16 is bonded to the conductor lines 2 and 9 provided on the surface of the

first-layer dielectric substrate 1. The ground metal 19 formed on the surface of the second-layer dielectric substrate 18 to which the semiconductor chip 16 is bonded is connected to ground metal 29 provided on the reverse side of the second-layer dielectric substrate 18 via through-holes in a part where the semiconductor chip 16 is bonded.

A part 35 of the ground metal 19 on the surface of the second-layer dielectric substrate 18 is removed so that a part opposite to the conductor line 9 of the matching circuit on the output side on the surface of the first-layer dielectric substrate 1 is included. The dielectric substrate in the removed part can be thicker than the first-layer dielectric substrate 1 or the second-layer dielectric substrate 18. The ground metal 19 is connected to the ground metal 29 formed on the reverse side of the second-layer dielectric substrate 18 via through-holes in the periphery of the dielectric substrate.

Sixth Embodiment

Fig. 15 is a block diagram showing a mobile wireless terminal equivalent to one embodiment of a communication device according to the invention. Fig. 16 is a part layout drawing showing a high frequency unit of the mobile wireless terminal shown in Fig. 15. A signal at the transmitting end is output from an antenna-2 102 via a modulator 108, a burst switch 107, a driving amplifier 106, a filter 105, a power

amplifier 104 and a duplexer 103. For a signal at the receiving end, a diversity system in which a case that a signal is received from an antenna-1 101 and is transmitted via a low noise amplifier 109, a filter 105, a frequency converter 110 and an IF amplifier 111 and a case that a signal is received from the antenna-2 102 and is transmitted via a low noise amplifier 109, a filter 105, a frequency converter 110 and an IF amplifier 111 are compared, a received signal is processed in a demodulation unit 113 and reaches a base band unit 114 is adopted. A reference number 112 denotes a frequency synthesizer.

The high frequency circuit module described in any of the first to fifth embodiments is used for the power amplifier 104 and a low noise amplifier 109. For the power amplifier 104, the high frequency circuit module that the dielectric substrate between the conductor line of the matching circuit on the input side and the ground metal is also composed of two or more layers is used in addition to the high frequency circuit module that the dielectric substrate between the conductor line of the matching circuit on the output side and the ground metal is composed of two or more layers.

For the low noise amplifier 109, the high frequency circuit module that the dielectric substrate between the conductor line of the matching circuit on the output side and the ground metal is also composed

of two or more layers is used in addition to the high frequency circuit module that the dielectric substrate between the conductor line of the matching circuit on the input side and the ground metal is composed of two or more layers. The mobile wireless terminal can be miniaturized by using these high frequency circuit modules.

Various other modifications, alternative, constructions and equivalents may be employed without departing from the true spirit scope off the invention, as exemplified in foregoing description and defined in the following claims.

What Is Claimed Is:

1. A high frequency circuit module provided with a two- or more-layer dielectric substrate, a semiconductor element and matching circuits on the input side and on the output side respectively of the semiconductor element respectively formed on the dielectric substrate, and ground metal, wherein:

a thickness of the dielectric substrate between a conductor of conductor line of said matching circuit on the output side and said ground metal is composed of two or more layers.

2. A high frequency circuit module according to Claim 1, wherein:

a thickness of the dielectric substrate between said conductor of conductor line of said matching circuit on the input side and said ground metal is composed of two or more layers.

3. A high frequency circuit module provided with a two- or more-layer dielectric substrate, a semiconductor element and matching circuits on the input side and on the output side respectively of the semiconductor element respectively formed on the dielectric substrate, and ground metal, wherein:

ground metal provided to the dielectric substrate existing between a conductor of transmission line of said matching circuit on the output side and said ground metal is formed in the shape in which a part is hollowed out so that a part opposite to said

conductor transmission line is included.

4. A high frequency circuit module according to Claim 3, wherein:

ground metal provided to the dielectric substrate existing between said conductor of transmission line of said matching circuit on the input side and said ground metal is formed in the shape in which a part is hollowed out so that a part opposite to said conductor of said transmission line is included.

5. A high frequency circuit module provided with a two- or more-layer dielectric substrate, a semiconductor element and matching circuits on the input side and on the output side respectively of the semiconductor element respectively formed on the dielectric substrate, and ground metal, wherein:

a thickness of the dielectric substrate between a conductor of transmission line of said matching circuit on the input side and said ground metal is composed of two or more layers.

6. A high frequency circuit module according to Claim 5, wherein:

a thickness of the dielectric substrate between said conductor of transmission line of said matching circuit on the output side and said ground metal is composed of two or more layers.

7. A high frequency circuit module provided with a two- or more-layer dielectric substrate, a semiconductor element and matching circuits on the

input side and on the output side respectively of the semiconductor element respectively formed on the dielectric substrate, and ground metal, wherein:

ground metal provided to the dielectric substrate existing between a conductor of transmission line of said matching circuit on the input side and said ground metal is formed in the shape in which a part is hollowed out so that a part opposite to said conductor of transmission line is included.

8. A high frequency circuit module according to Claim 7, wherein:

ground metal provided to the dielectric substrate existing between said conductor of transmission line of said matching circuit on the output side and said ground metal is formed in the shape in which a part is hollowed out so that a part opposite to conductor of said transmission line is included.

9. A communication device, wherein:

the high frequency circuit module according to Claim 1 is used for a power amplifier at the transmitting end.

10. A communication device, wherein:

the high frequency circuit module according to Claim 2 is used for the power amplifier at the transmitting end.

11. A communication device, wherein:

the high frequency circuit module according to

Claim 3 is used for the power amplifier at the transmitting end.

12. A communication device, wherein:

the high frequency circuit module according to Claim 4 is used for the power amplifier at the transmitting end.

13. A communication device, wherein:

the high frequency circuit module according to Claim 5 is used for a low noise amplifier at the receiving end.

14. A communication device, wherein:

the high frequency circuit module according to Claim 6 is used for the low noise amplifier at the receiving end.

15. A communication device, wherein:

the high frequency circuit module according to Claim 7 is used for the low noise amplifier at the receiving end.

16. A communication device, wherein:

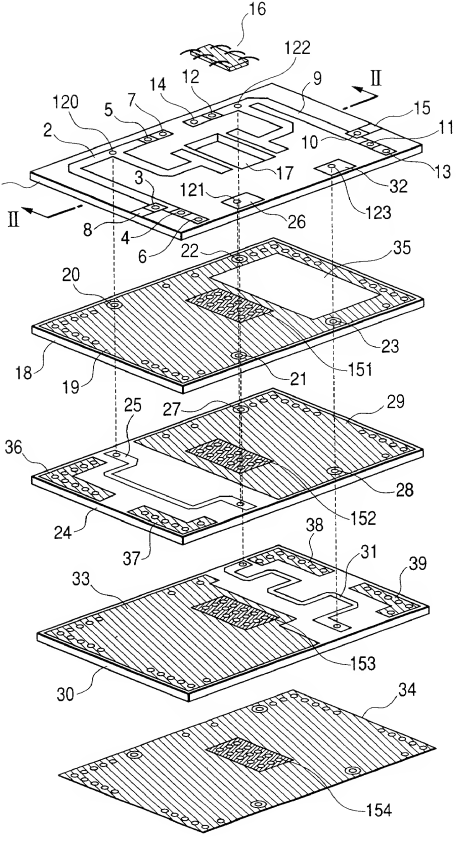
the high frequency circuit module according to Claim 8 is used for the low noise amplifier at the receiving end.

ABSTRACT

The invention relates to a high frequency circuit module in which a two- or more-layer dielectric substrate is used, the dielectric substrate between a conductor line of a matching circuit on the input side or on the output side and ground metal is composed of two or more layers and the miniaturization is enabled and a communication device using it.

As a required part can be thickened without changing the thickness of the whole dielectric substrate, the transmission loss can be reduced and the miniaturization of the high frequency circuit module and the communication device using it is enabled.

FIG. 1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122
12
14
9
II
120
5
7
15
2
11
10
17
13
1
3
121
32
123
II
26
8
4
6
22
35
20
23
18
19
21
151
25
27
29
36
28
152
24
37
38
31
39
33
153
30
34
154

FIG. 2

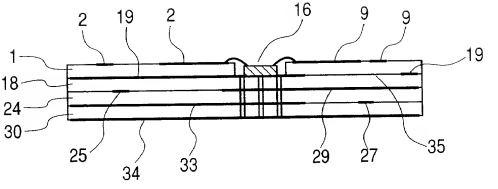

2
19
2
16
9
9
19
1
18
24
30
25
34
33
29
27
35

FIG. 3

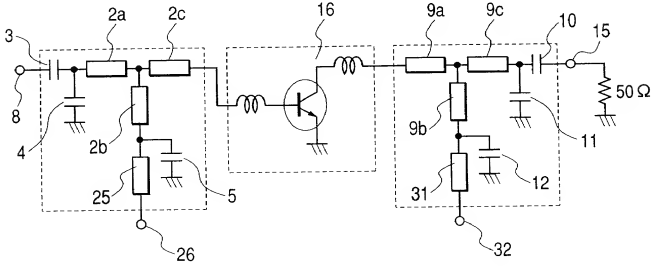

3
2a
2c
16
9a
9c
10
15
50 Ω
8
4
2b
9b
11
25
5
31
12
26
32

FIG. 4

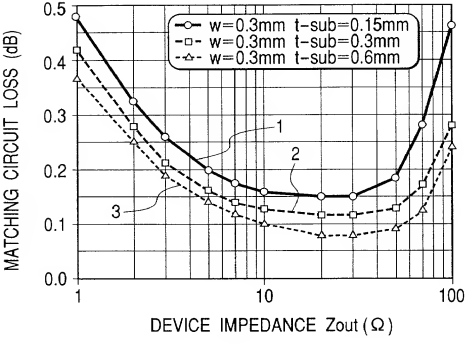
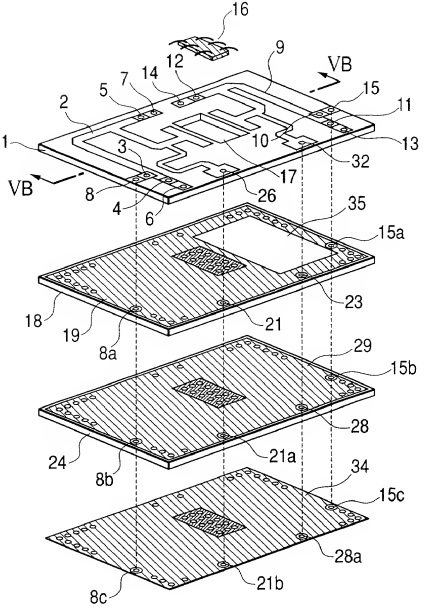

w=0.3mm t-sub=0.15mm
w=0.3mm t-sub=0.3mm
w=0.3mm t-sub=0.6mm
MATCHING CIRCUIT LOSS (dB)
0.5
0.4
0.3
0.2
0.1
0.0
1
10
100
DEVICE IMPEDANCE Zout (Ω)
1
2
3

FIG. 5A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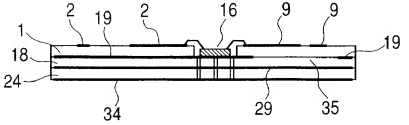
9
12
VB
14
7
5
15
2
11
10
13
1
3
32
17
VB
8
26
4
6
35
15a
23
18
19
21
8a
29
15b
28
24
21a
8b
34
15c
28a
21b
8c

FIG. 5B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2
16
9
9
1
19
18
24
34
29
35

FIG. 6A

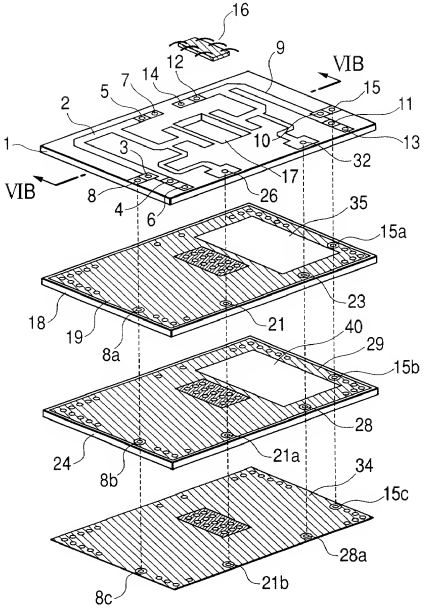


FIG. 6B

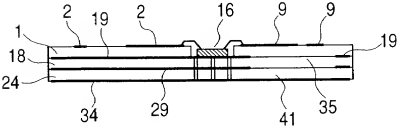


FIG. 7A

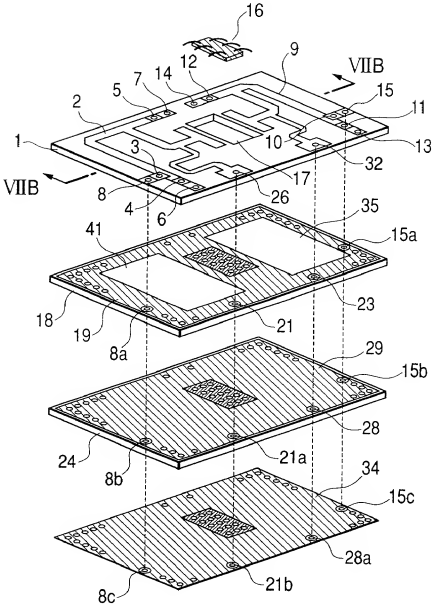
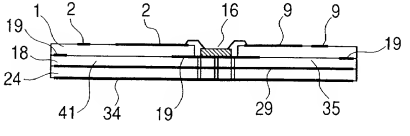

16
12
9
VIIB
14
7
5
15
2
11
1
10
3
13
32
17
VIIB
8
26
4
6
35
41
15a
18
23
19
21
8a
29
15b
28
24
21a
8b
34
15c
28a
8c
21b

FIG. 7B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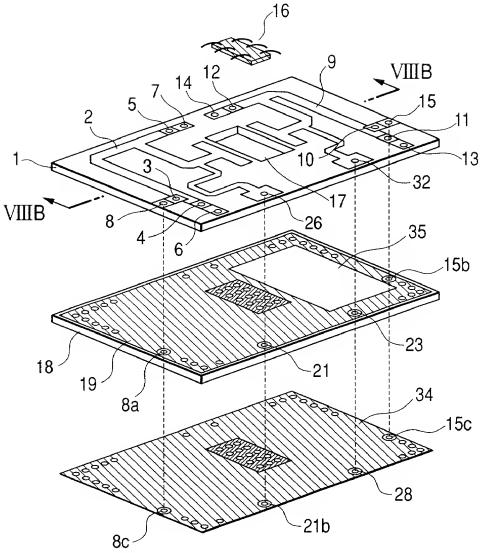
1
2
2
16
9
9
18
19
24
41
34
19
29
35

FIG. 8A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12
9
VIIIB
14
7
15
5
11
2
10
13
1
3
32
17
VIIIB
8
26
4
6
35
15b
18
23
19
21
8a
34
15c
28
21b
8c

FIG. 8B

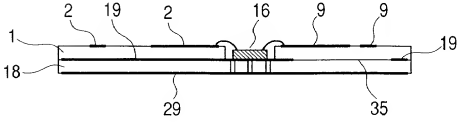

2
19
2
16
9
9
1
19
18
29
35

FIG. 9

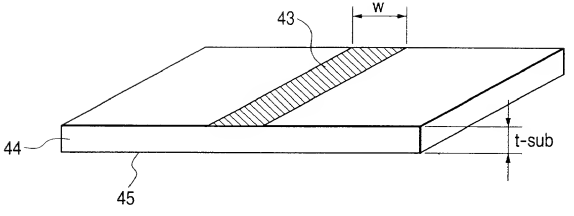

w
43
t-sub
44
45

FIG. 10

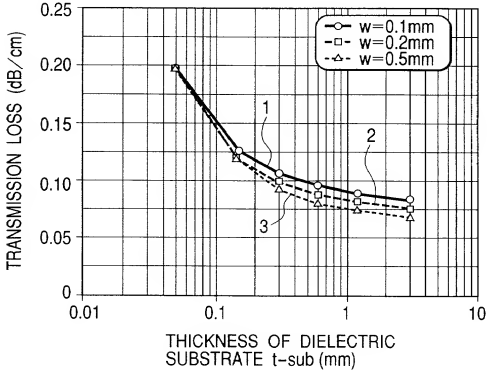

w=0.1mm
w=0.2mm
w=0.5mm
1
2
3
TRANSMISSION LOSS (dB/cm)
0.25
0.20
0.15
0.10
0.05
0
0.01
0.1
1
10
THICKNESS OF DIELECTRIC SUBSTRATE t-sub (mm)

FIG. 11

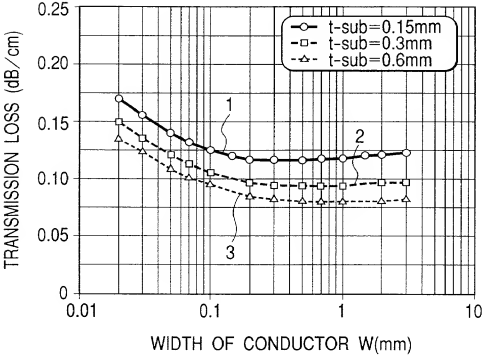

0.25
0.20
0.15
0.10
0.05
0
TRANSMISSION LOSS (dB/cm)
t-sub=0.15mm
t-sub=0.3mm
t-sub=0.6mm
1
2
3
0.01
0.1
1
10
WIDTH OF CONDUCTOR W(mm)

FIG. 12

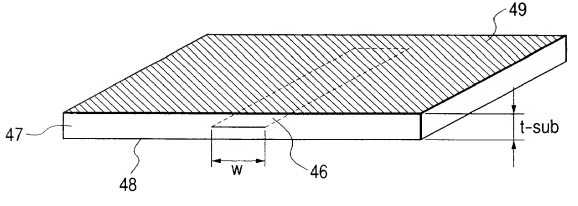

49
47
t-sub
w
46
48

FIG. 13

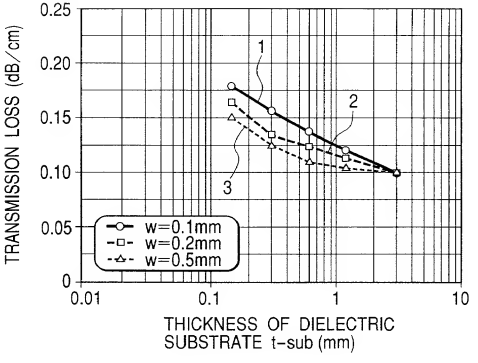

TRANSMISSION LOSS (dB/cm)
0.25
0.20
0.15
0.10
0.05
0
0.01
0.1
1
10
1
2
3
w=0.1mm
w=0.2mm
w=0.5mm
THICKNESS OF DIELECTRIC SUBSTRATE t-sub (mm)

FIG. 14

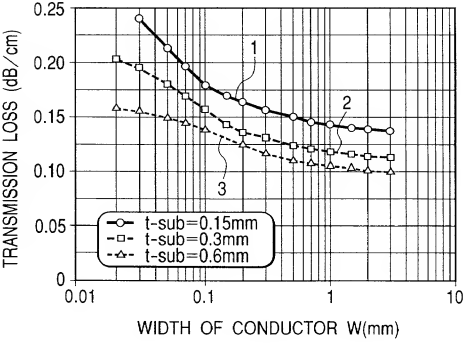

TRANSMISSION LOSS (dB/cm)
0.25
0.20
0.15
0.10
0.05
0
0.01
0.1
1
10
1
2
3
t-sub=0.15mm
t-sub=0.3mm
t-sub=0.6mm
WIDTH OF CONDUCTOR W(mm)

FIG. 15

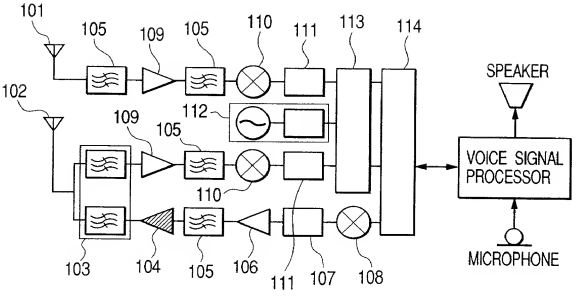
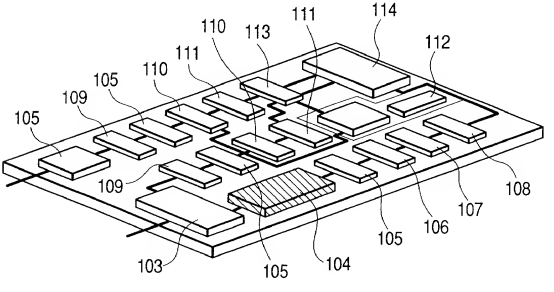

101
105
109
105
110
111
113
114
102
112
109
105
110
SPEAKER
VOICE SIGNAL PROCESSOR
MICROPHONE
103
104
105
106
111
107
108

FIG. 16


110
113
111
114
111
112
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105
109
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108
107
106
105
103
105
104

N70149US (キ)

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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH FREQUENCY CIRCUIT MODULE AND
COMMUNICATION DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を__________とし、(該当する場合) __________に訂正されました。

☐ was filed on __________ as United States Application Number or PCT International Application Number __________ and was amended on __________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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(日本語宣言書)

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
１１－２７５７３０	Ｊａｐａｎ	２９／Ｓｅｐｔｅｍｂｅｒ／１９９９	☐
			☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

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Daniel J. Stanger, Reg. No.32,846
Shrinath Malur, Reg. No.34,663;
Gene W. Stockman, Reg. No.21,021
Jeffrey M. Ketchum, Reg. No.31,174;
and Scott W. Brickner, Reg. No.34,553.

書類送付先

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104 East Hume Avenue
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Telephone: (703) 684-1120
Fax: (703) 684-1157

唯一または第一発明者名	Full name of sole or first inventor Eiichi HASE
発明者の署名 日付	Inventor's signature Date Eiichi Hase 7/25/2000
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国籍	Citizenship Japan
私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

（第二以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for second and subsequent joint inventors.)

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第二共同発明者名	Full name of second joint inventor, if any Shun IMAI
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第四共同発明者の署名　　日付	Fourth inventor's signature　　Date
住所	Residence
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第五共同発明者名	Full name of fifth joint inventor, if any
第五共同発明者の署名　　日付	Fifth inventor's signature　　Date
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